IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 11 and 27-30 in accordance with the following:

1-10 (CANCELLED)

11. (CURRENTLY AMENDED) A processor execution pipeline, comprising:

a first instruction decoding unit that determines at least a kind of instruction, decodes a first instruction into a first control signal, and decodes all other instructions with the exception of the first instruction into a second control signal upon determining at least the kind of instruction;

a first processing unit that performs a first operation on a first data when receiving the first control signal, and passes through the first data when receiving the second control signal;

a second instruction decoding unit that determines at least a kind of instruction, decodes a second instruction into a third control signal, and decodes all other instructions with the exception of the second instruction into a fourth control signal upon determining at least the kind of instruction;

a second processing unit that performs a second operation on a second data when receiving the third control signal, ~~where~~ the second data ~~is~~ being an output of the first processing unit; and

a multiplexer that selects an output of the second processing unit or the second data, wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage.

12. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 11, wherein

the multiplexer selects an output of the second processing unit when receiving the third control signal, and selects the second data when receiving the fourth control signal.

13. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 11, further comprising:

a latching unit that holds the output of the first processing unit where the second data is data held by the latching unit.

14. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 11, wherein the first processing unit receives multiple data as the first data.

15. (PREVIOUSLY PRESENTED) A processor execution pipeline, comprising:

a first instruction decoding unit that determines at least a kind of instruction, that decodes a first instruction into a first control signal, and that decodes all other instructions with the exception of the first instruction into a second control signal upon determining at least the kind of instruction;

a first processing unit that performs a first operation on a first data when receiving the first control signal;

a multiplexer that selects an output of the first processing unit or the first data;

a second instruction decoding unit that determines at least a kind of instruction, that decodes a second instruction into a third control signal, and decodes all other instructions with the exception of the second instruction into a fourth control signal upon determining at least the kind of instruction; and

a second processing unit that performs a second operation on a second data when receiving the third control signal, and passes the second data when receiving the fourth control signal, where the second data is an output of the multiplexer.

16. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 15, wherein

the multiplexer selects an output of the first processing unit when receiving the first control signal, and selects the first data when receiving the second control signal.

17. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 15, further comprising:

a latching unit that holds the output of the multiplexer, where the second data is data held by the latching unit.

18. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 15, wherein

the first processing unit receives multiple data as the first data, and the multiplexer receives the output of the first operating unit and one of the multiple data.

19. (CURRENTLY AMENDED) A processor execution pipeline, comprising:

a first instruction decoding unit that determines at least a kind of instruction, that decodes a first instruction into a first control signal, and that decodes all other instructions with the exception of the first instruction into a second control signal upon determining at least the kind of instruction;

a first processing unit that performs a first operation on a first data when receiving the first control signal, and passes the first data when receiving the second control signal;

a second instruction decoding unit that determines at least a kind of instruction, that decodes the first instruction into a third control signal, decodes a second instruction into a fourth control signal, and decodes all other instructions with the exception of the first and second instructions into a fifth control signal upon determining at least the kind of instruction;

a second processing unit that performs a second operation on a second data when receiving the third control signal, and performs a third operation on the second data when receiving the fourth control signal, where the second data is an output of the first processing unit; and

a multiplexer that selects an output of the second processing unit or the second data, wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage.

20. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 19, wherein

the multiplexer selects an output of the second processing unit when receiving either one of the third or the fourth control signals, and selects the second data when receiving the fifth control signal.

21. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim

19, further comprising:

a latching unit that holds the output of the first processing unit, where the second data is data held by the latching unit.

22. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 19, wherein the first processing unit receives multiple data as the first data.

23. (CURRENTLY AMENDED) A processor execution pipeline, comprising:

a first instruction decoding unit that determines at least a kind of instruction, that decodes a first instruction into a first control signal, decodes a second instruction into a second control signal, and decodes all other instructions with the exception of the first and second instructions into a third control signal upon determining at least the kind of instruction;

a first processing unit that performs a first operation on a first data when receiving the first control signal, and performs a second operation on the first data when receiving the second control signal;

a multiplexer that selects an output of the first processing unit or the first data;

a second instruction decoding unit that decodes the first instruction into a fourth control signal, and decodes all other instructions with the exception of the first instruction into a fifth control signal upon determining at least the kind of instruction; and

a second processing unit that performs a third operation on a second data when receiving the fourth control signal, and passes the second data when receiving the fifth control signal, where the second data is an output of the multiplexer, wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage.

24. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 23, wherein

the multiplexer selects an output of the first processing unit when receiving either one of the first or the second control signals, and selects the first data when receiving the third control signal.

25. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 23, further comprising:

a latching unit that holds the output of the multiplexer, where the second data is data held by the latching unit.

26. (PREVIOUSLY PRESENTED) The processor execution pipeline according to claim 23, wherein

the first processing unit receives multiple data as the first data, and

the multiplexer receives the output of the first operating unit and one of the multiple data.

27. (CURRENTLY AMENDED) A processor execution pipeline having at least a latching unit to hold and output data, comprising:

a first instruction decoding unit to convert a first instruction into a first control signal, and to convert all other instructions with the exception of the first instruction into a second control signal;

a first processing unit to perform a first operation on a first data when receiving the first control signal, and to pass the first data when receiving the second control signal;

a second instruction decoding unit to convert a second instruction into a third control signal, and to convert all other instructions with the exception of the second instruction into a fourth control signal;

a second processing unit to perform a second operation on a second data when receiving the third control signal where the second data is an output of the first processing unit; and

a multiplexer that selects an output of the second processing unit or the second data;

wherein the latching unit holds an output of the first processing unit and the second data is held by the latching unit allowing the latching unit to be shared by the first and second processing units, and the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage.

28. (CURRENTLY AMENDED) A processor execution pipeline method, comprising:

decoding a first instruction into a first control signal, and decoding all other instructions with the exception of the first instruction into a second control signal;

performing a first operation on a first data when receiving the first control signal and passing the first data when receiving the second control signal via a first processing unit;

decoding a second instruction into a third control signal, and decoding all other instructions with the exception of the second instruction into a fourth control signal;

performing a second operation on a second data via a second processing unit when receiving the second control signal, where the second data is an output of the first processing unit; and

selecting an output of the second processing unit or the second data, wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage.

29. (CURRENTLY AMENDED) A processor execution pipeline method, comprising:

decoding a first instruction into a first control signal and all other instructions into a second control signal, and decoding a second instruction into a third control signal and all other instructions with the exception of the second instruction into a fourth control signal; and

first and second processing units respectively executing first and second instructions using data held in a latching unit, wherein each instruction is decoded to pass the data held in the latching unit through the first processing unit, and the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage.

30. (CURRENTLY AMENDED) A processor execution pipeline method, comprising:

decoding a first instruction in a first processing stage into a first control signal and decoding all other instructions in the first processing stage into a second control signal, and decoding a second instruction in a second processing stage into a third control signal and all other instructions in the second processing stage into a fourth control signal; and

executing a first operation on a first data upon receipt of the first control signal and holding a result of the execution of the first operation until receipt of the second control signal;

executing a second operation on the result of the execution of the first operation when receiving the third control signal and holding a result of the execution of the second operation until receipt of the fourth control signal; and

selecting the result of the first operation or the second operation as an output, where the first instruction and the second instruction are unrelated to one another, wherein the first, second and all other instructions are selectively decoded based on whether operations are to be performed thereto in a current processing stage or passed through data to a next stage.